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Sub B1 ~~SEMICONDUCTOR PACKAGE INCLUDING LEADS WITH VERTICALLY DOWNSET INNER ENDS~~

INVENTOR

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CROSS-REFERENCE TO RELATED APPLICATIONS
(Not Applicable)

STATEMENT RE: FEDERALLY SPONSORED RESEARCH/DEVELOPMENT
(Not Applicable)

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates generally to semiconductor packages, and more particularly to a semiconductor package which includes leads with vertically downset inner ends.

2. Description of the Related Art

[0002] The current trend in the electronics industry is to provide electronic appliances which are multi-functional, compact, and capable of achieving high performance levels. In view of this trend, a requirement has arisen that the semiconductor packages which are used in such electronic appliances be made in a "chip size". These chip-size packages are often referred to as a chip scale package or CSP. These chip-sized small semiconductor packages are usable in portable products such as cellular phones and PDA's which require high levels of reliability, electrical efficiency, and a small or compact size of

minimal weight.

[0003] One type of currently manufactured CSP is a very small semiconductor package including a lead frame. This particular type of semiconductor package is constructed in a manner wherein a plurality of input/output signal lands (e.g. from four to one hundred signal lands) are formed at the edge of the bottom surface of the package. This package is electrically connected to a printed circuit board by soldering the lands on the bottom surface of the package. This configuration is in contrast to conventional lead frame packages which include, as an alternative to these signal lands, leads which project outwardly from the package and are formed by various trimming/forming techniques. In addition to including the signal lands formed at the periphery of the bottom surface thereof, these semiconductor packages also include a chip mounting pad, the bottom surface of which is exposed for purposes of maximizing an emission rate of heat generated by a semiconductor chip mounted thereto.

[0004] Internal to such semiconductor package is a semiconductor chip with a multitude of input/output pads. Such pads are in turn connected to leads which terminate at the signal lands. An overall limitation of the semiconductor chip design as well as the semiconductor package has been the electrical connections and configurations utilized to satisfy the required electrical inputs and outputs to and from the input/output pads. In addition, though the above-described semiconductor packages provide the small size required by the electronic appliances discussed above, they possess certain deficiencies which detract from their overall utility. One such deficiency is insufficient bonding strength between the lead frame and the remainder of the semiconductor package. The lack of adequate bonding strength makes the

semiconductor package vulnerable to failure attributable to the creation of electrical discontinuities and/or the dislodging of one or more of the signal lands of the lead frame from the remainder of the semiconductor package. Accordingly, there is a need in the art for an improved semiconductor package design.

BRIEF SUMMARY OF THE INVENTION

[0005] In accordance with an aspect of the present invention, there is provided a semiconductor package which includes a chip mounting pad having a peripheral edge. The package further includes a semiconductor chip attached to the chip mounting pad. The package further includes a plurality of leads. Each lead includes an inner end and an opposing distal end. Each inner end is disposed adjacent the peripheral edge in spaced relation thereto and vertically downset with respect to each respective distal end. The package further includes at least one isolated ring structure disposed along the peripheral edge between the peripheral edge and the inner ends of the leads in spaced relation thereto. The ring structure is electrically connected to the semiconductor chip and an inner end of at least one of the leads.

[0006] Advantageously, the vertically downset nature of the inner ends of the leads (i.e., the inner ends being offset from the distal ends) tend to enhance the bonding strength of the leads with respect the overall semiconductor package. In this regard, the inner ends being vertically downset or offset enables encapsulation of the inner ends with a sealing part for securing the same internally within the semiconductor package. As such, this enhanced bonding strength tends to substantially eliminate occurrences of delamination between such sealing part and the remainder of the lead frame, such as the inadvertent

dislodging of the distal ends (i.e., signal lands) from the sealing part thereby maintaining the overall integrity of the semiconductor package.

[0007] According to respective embodiments, each inner end is vertically downset with respect to each respective distal end a distance approximately equal to a thickness of the leads. The semiconductor chip includes a chip top surface and the inner ends each include an inner end top surface, and the inner end top surfaces are aligned with the chip top surface. The ring structure includes a ring top surface and the inner ends each include an inner end top surface, and the inner end top surfaces are aligned with the ring top surface. Each inner end is vertically downset with respect to each respective distal end via a die press operation. The leads each further include a lead transition section disposed between the respective inner and distal ends. The lead transition sections are angularly disposed with respect to the distal ends. The semiconductor package is contemplated to further include a sealing part which encapsulates at least the inner ends of the leads.

[0008] The present invention is best understood by reference to the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] These, as well as other features of the present invention, will become more apparent upon reference to the accompanying drawings wherein:

[0010] Figure 1 is a top plan view of a lead frame including a chip mounting pad, ring structures and leads of a semiconductor package constructed in accordance with an aspect of the present invention;

[0011] Figure 2 is an enlargement of the encircled region of the lead frame as shown in Figure 1;

[0012] Figure 3 is the region of the lead frame as shown in Figure 2 with the ring structure formed from the lead frame with the removal of connecting bars, a nonconductive connector the ring structure and leads, and a semiconductor chip;

[0013] Figure 4 is the region of the lead frame as shown in Figure 3 with electrical connections among the semiconductor chip, the ring structure, and the leads.

[0014] Figure 5 is a cross sectional view of a completed semiconductor package including the lead having a downset inner end as seen along axis 5-5 of Figure 4;

[0015] Figure 6 is a cross sectional view of a completed semiconductor package as seen along axis 6-6 of Figure 4; and

[0016] Figure 7 is a cross sectional view of a completed semiconductor package as seen along axis 7-7 of Figure 4.

[0017] Common reference numerals are used throughout the drawings and detailed description to indicate like elements.

DETAILED DESCRIPTION OF THE INVENTION

[0018] Referring now to the drawings wherein the showings are for purposes of illustrating preferred embodiments of the present invention only, and not for purposes of limiting the same, Figures 1-8 illustrate semiconductor packages and methods of fabricating the same according to aspects of the present invention.

[0019] Lead frames for semiconductor packages are typically manufactured by mechanically stamping or chemically etching a continuous metal strip. The lead frame serves as a lead connecting a semiconductor chip to

an external circuit such as a printed circuit board. The lead frame further serves as a frame for fixing the semiconductor package to the printed circuit board while providing an electrical connection between the printed circuit board and the semiconductor chip.

[0020] According to an aspect of the present invention, a lead frame 10 is initially provided in a method of fabricating a semiconductor package 12 (as shown in Figure 6). Figure 1 is a top plan view of the lead frame 10. The lead frame 10 includes a frame 14 which is a substantially flat or planar plate defining a centrally located space 16. Disposed within the space 16 is a chip mounting pad 18 of the lead frame 10. The chip mounting pad 18 is a substantially square plate which is connected to the frame 14 by a plurality of tie bars 20. Four (4) tie bars 20 are used to connect the chip mounting pad 18 to the frame 14, with the tie bars 20 extending from respective ones of the four corner regions defined by the chip mounting pad 18. The tie bars 20 facilitate the stable support of the chip mounting pad 18 inside of the frame 14, and more particularly within the space 16 defined thereby.

[0021] The lead frame 10 further includes a plurality of leads 22 which extend from the frame 14 into the space 16 toward the chip mounting pad 18. A total of seventy-two leads 22 are included in the lead frame 10, with the leads 22 being segregated into four sets of eighteen, and each set of eighteen being disposed in spaced relation to a respective one of the four peripheral edge segments 24 of a peripheral edge 26 defined by the chip mounting pad 18. The leads 22 are each connected to and extend angularly from dambars 28. A total of four dambars 28 are shown in lead frame 10, with each set of eighteen leads 22 extending from a respective dambar 28 and terminating at an inner end 30. Thus, the leads 22 are supported in a stable manner in

the space 16 defined by the frame 14 by the dambars 28.

[0022] Those of ordinary skill in the art will recognize that the position and path of the leads 22 may be varied, and that the leads 22 can be suitably designed according to the number and position of input/output paths desired in the semiconductor package 12. Additionally, though the lead frame 10 is shown as a square configuration, it may alternatively be rectangularly configured. Similarly, though the chip mounting pad 18 is shown as being generally square, the same may also be provided in a generally rectangular configuration. Further, though the leads 22 are shown as being formed in four separate sets around the peripheral edge 26 of the chip mounting pad 18, the leads 22 may also be provided in only two sets extending along and in spaced relation to respective ones of only two of the peripheral edge segments 24 of the chip mounting pad 18. Still further, the chip mounting pad 18 may be connected to the frame 14 through the use of only two tie bars 20 as opposed to the four tie bars 20 as shown.

[0023] The lead frame 10 further includes at least one isolated ring structure 32. In the embodiment shown, four ring structures 32 are disposed along respective ones of the four peripheral edge segments 24 of the chip mounting pad 18 between the peripheral edge 26 and the inner ends 30 of the leads 33 in spaced relation thereto. In this regard, the ring structures 32 collectively form a "ring" about the chip mounting pad 18.

[0024] Referring additionally to Figure 2 there is depicted an enlargement of the encircled region of the lead frame 10 as shown in Figure 1. Each ring structure 32 includes a main body portion 34 which is disposed along a respective peripheral edge segment 24. The main body portion 34 includes an intermediate section 36 which is bounded by opposing end sections 38, 40. The main body

portion 34 is disposed between the inner ends 30 of the leads 22 and the peripheral edge segments 24. With the exception of temporary connecting bars 48 described below, the main body portion 34 is disposed in spaced relation to inner end surfaces 96 of the inner ends 30 of the leads 22 and the peripheral edge segments 24 (as additionally depicted in the completed semiconductor package 12 of Figure 5, as seen respectively along axis 5-5 of the Figure 4).

[0025] The ring structure 32 further includes at least one stub portion, such as first, second and third stub portions 42, 44, 46. Additional or fewer stub portions may be included. The first and second stub portions 42, 44 extend distally respectively from the end sections 38, 40. The first and second stub portions 42, 44 may angularly extend from the main body portion 34. Each of the first and second stub portions 42, 44 extend between a given tie bar 20 and an adjoining lead 22. The third stub portion 46 extends laterally from the intermediate section 36 away from the peripheral edge segment 24 along and between a pair of the leads 22.

[0026] Two pairs of temporary connecting bars 48, 50 are utilized to support the ring structure 32 within the frame 14 and to maintain the ring structure 32 in fixed relation to the chip mounting pad 18 and the leads 22 during fabrication of the semiconductor package 12. In the embodiment shown, two temporary connecting bars 48 extend between selected ones of the leads 22 (specifically leads 22a) and the intermediate section 36, and two temporary connecting bars 50 extend between the intermediate section 36 and the adjacent peripheral edge segment 24.

[0027] It is contemplated that additional or fewer temporary connecting bars 48, 50 may be utilized to connect the ring structure 32 to the frame 14. For example, though

not shown, connecting bars 48 may extend from any one of the stub portions 42, 44, 46. Thus, the ring structure 32 need not be directly connected to the chip mounting pad 18 and the leads 22, but may none the less be connected via connecting bars to other structures of the frame 14. Further, the temporary connecting bars 48, 50 are not required to connect to the chip mounting pad 18 or the leads 22 as shown, but may be attached to other structures connected to the frame 14, such as the tie bars 20 or the dambars 28. While the ring structure 32 and temporary connecting bars 48, 50 are shown to have a different hatch patterns from that of the chip mounting pad 18, the tie bars 20, and the leads 22 it is understood that such structures are formed from a contiguous sheet of material of the lead frame 10, as the such different hatch patterns are only utilized for ease of identification.

[0028] The lead frame 10 may be manufactured from a sheet of metal material, such as copper (Cu), copper alloy (Cu Alloy), alloy 37 (nickel (Ni) of 37%, iron (Fe) of 55%). The lead frame 10 may have a uniform thickness of about 0.25 millimeters (about 10 mils). Such thickness is exemplary only, and can be varied according to the application field. Moreover, it is contemplated that the lead frame 10 need not have a uniform thickness. For example, selective portions of such components, such as the peripheral portion of the chip mounting pad 18 may be undercut via etching for improved encapsulant adhesion during later stages of the fabrication of the semiconductor package 12.

[0029] Finally, the lead frame 10 may be plated with a conductive metal, such as gold (Au), silver (Ag), nickel (Ni), palladium (Pd), or alloys thereof, as a surface preparation to facilitate bonding as discussed below.

[0030] Having thus initially provided the above

described lead frame 10, the method of fabrication further provides for attachment of a nonconductive connector 51 as shown in Figure 3. As will be discussed further below, the leads 22 are later formed to each include distal ends 68 opposite the inner ends 30. Moreover, transition sections 92 are formed between the inner and distal ends 30, 68. The nonconductive connector 51 is attached to the distal ends 68 of the leads 22 and the stub portions 42, 44, 46 for maintaining the ring structure 32 in fixed relationship to the chip mounting pad 18 and the leads 22. In particular, the nonconductive connector 51 is attached to distal end top surfaces 82 of the distal ends 68 of the leads 22 and the top surfaces of stub portion distal sections 58. For additional support, the nonconductive connector 51 may be further attached to the tie bars 20. The nonconductive connector 51 may be adhesive tape, such as a conventional polyimide-based tape. Dedicated equipment may be utilized which punches out a piece of tape from a reel in the desired pattern using a custom tape punch tool. The nonconductive connector 51 is then placed upon the lead frame 10, and in particular across the stub portions 42, 44, 46, using an automated pick and place apparatus.

[0031] The method further provides for removing the temporary connecting bars 48, 50. Having removed the temporary connecting bars 48, 50, the ring structure 32 is contemplated to be electrically isolated in nature from the chip mounting pad 18, the leads 22, the tie bars 20, and any other portion of the frame 14. The removal of the temporary connecting bars 48, 50 may be accomplished via a punch process wherein a standard punch and die set are configured to remove each of the connecting bars 48, 50. The nonconductive connector 51 is sized and configured to provided sufficient stabilization to maintain the ring

structure 32 in a fixed relationship with the chip mounting pad 18 and the leads 22 during this removal process of the temporary connecting bars 48, 50.

[0032] Referring now to Figure 4, portions of the frame 12 are downset such as through a die press operation. In particular, the inner ends 30 of the leads 22 and the main body portion 34 of the ring structure 32 are formed to be vertically raised or off-set from those other portions of the frame 12. Such downsetting results in each inner end 30 being vertically downset or offset with respect to each respective distal end 68. The transition sections 92 of the leads 22 are thus formed between the inner ends 30 and the distal ends 68 (as additionally depicted in the completed semiconductor package 12 of Figures 5 and 7, as seen respectively along axes 5-5 and 7-7 of Figure 4).

[0033] In addition, the downsetting results in the stub portions 42, 44, 46 of the ring structure 32 each including the stub portion distal section 58 vertically downset or offset from the main body portion 34. Stub portion transition sections 60 are thus formed between the stub portion distal sections 58 and the main body portion 34 (as additionally depicted in the completed semiconductor package 12 of Figure 6, as seen along axis 6-6 of Figure 4). The location and placement of the nonconductive connector 51 is such that the nonconductive connector 51 extends across the distal ends 68 of the leads 22, the stub portion distal sections 58 and the tie bars 20.

[0034] Each inner end 30 may be vertically downset with respect to each respective distal end 68 a distance approximately equal to a thickness of the leads 22. The inner ends 30 include the inner end top surfaces 78 and opposing inner end bottom surfaces 80, and the distal ends 68 include distal end top surfaces 82 and opposing distal end bottom surfaces or signal lands 72. As mentioned

above, the lead frame 10 may be formed of a sheet of material having a thickness of about 0.25 millimeters (about 10 mils). As such the leads 22 may be bent during the downsetting process such that the inner end top surfaces 78 are offset from the distal end top surfaces 82 by about 0.25 millimeters. Stated otherwise, the inner end bottom surfaces 80 may be aligned with the distal end top surfaces 82. It is understood that such offset distance is exemplary.

[0035] It is contemplated that the downsetting of the leads 22 may be effectuated such that the inner ends 30 are aligned with other portions of the semiconductor package 12. In this regard, the completed semiconductor package 12 includes a semiconductor chip 52 as discussed below. Such semiconductor chip 52 includes a chip top surface 94. The semiconductor chip 52 is mounted upon the chip mounting pad 18. The inner end top surfaces 78 may be aligned with (i.e., coplanar to) the chip top surface 94. Moreover, as the ring structure 32 may be downset along with the leads 22, the inner end top surfaces 78 may be aligned with (i.e., coplanar to) an intermediate section top surface 84 of the intermediate section 36 of the ring structure 32. Thus, the intermediate section 36 may include an intermediate section bottom surface 86 aligned with the inner end bottom surfaces 80.

[0036] Additionally, the angular disposition of the transition sections 92 may be varied. For example, the transition sections 92 may be disposed at an angle in the range of thirty degrees to forty-five degrees with respect to the distal ends 68. It is understood that while the transition sections 92 are shown to have well defined angulations with respect to the contiguously formed inner and distal ends 30, 68, the transitions between the transition sections 92 and the inner and distal ends 30, 92

may be more curved in nature than as depicted. Moreover, the lengths of the inner ends 30, transition sections 92 and distal ends 68 may be varied as well.

[0037] The method next provides for attaching a semiconductor chip 52 to the chip top surface 94 of the chip mounting pad 18. As mentioned above, the inner end top surfaces 78 may be vertically aligned with the chip top surface 94. As such, the inner ends 30 in this embodiment would be offset or downset by a thickness of the semiconductor chip 52 and any thickness associated with a bonding layer between the semiconductor chip 52 and a mounting pad top surface 74. Such attachment or bonding may be accomplished through the use of an epoxy, an adhesive film, or adhesive tape. The semiconductor chip 52 includes a plurality of input/output pads 54 disposed on the chip top surface 94.

[0038] The method further provides for electrically connecting the semiconductor chip 52 to the ring structure 32. In this regard, selected ones of the input/output pads 54, such as 54a, are electrically connected to the ring structure 32. In turn, the ring structure 32 is electrically connected to an inner end 30 of at least one of the leads 22, such as lead 22a. Such electrical connections may be facilitated through the use of conductive wires 56 (exemplary ones depicted). The conductive wires 56 may be formed of gold, copper, or aluminum wires for example. Moreover, common wire bonding techniques may be employed such as Au ball bonding. Thus, the conductive wire 56a is used to electrically connect the input/output pad 54a to the ring structure 32 (as additionally depicted in the completed semiconductor package 12 of Figure 6, as seen along axis 6-6 of Figure 4).

[0039] Further, the conductive wire 56b is used to

electrically connect the ring structure 32 to the inner end top surface 78 of lead 22a (as additionally depicted in the completed semiconductor package 12 of Figure 7, as seen along axis 7-7 of Figure 4). The forgoing configuration advantageously allows the ring structure 32 to share a common electrical potential as the connected lead 22a. For example, the lead 22a may be utilized for connection to an external power source (not shown). Connection of the lead 22a to the ring structure 32 is achieved through the connecting wire 56b. This in turn results in the entire ring structure 32 being conveniently available for connection by any of the input/output pads 54, such as pads 54a, through the connecting wires 56a. Thus, a single lead, lead 22a, may be utilized to power two of the input/output pads 54, thereby avoiding one-to-one dedication of leads 22 for each of the input/output pads 54. In an alternate exemplary usage, the lead 22a may be connected to electrical ground, thereby providing the ring structure 32 as a convenient ground source. In this embodiment, because the main body portion 34 of the ring structure 32 is similarly downset as the inner ends 30, this allows for ease of the electrical connection therebetween with the connecting wire 56b.

[0040] Referring additionally to the completed semiconductor package 12 of Figure 5, as seen along axis 5-5 of Figure 4, other ones of the input/output pads 54 of the semiconductor chip 52 are directly electrically connected other respective ones of the leads 22 through the connecting wires 56. In particular, connection is made to the inner end top surface 78. In this embodiment, because the chip top surface 94 is aligned with the inner end top surface 78, this allows for ease of the electrical connection therebetween with the connecting wire 56.

[0041] Thus, the electrical signals of the semiconductor

chip 52 can be transmitted to a printed circuit board (not shown) via the conductive wires 56 and the leads 22. The conductive wires 56 and the leads 22 may also be used to facilitate the transmission of electrical signals from the printed circuit board to the semiconductor chip 52.

[0042] In addition, the selected ones of the input/output pads 54, such pads 54b, may be electrically connected via conductive wires 56c to the chip mounting pad 18. It is contemplated that during operation of the semiconductor package 12, the chip mounting pad 18 may be electrically grounded by connection of a given one of the tie bars 20 to electrical ground.

[0043] It is contemplated that proscribed portions of the frame 12 are subsequently encapsulated. In this regard, the semiconductor chip 52, the chip mounting pad 18, the conductive wires 56, the tie bars 20, the leads 22 (including the inner ends 30) and the ring structure 32 are sealed with a sealing material, such as an epoxy molding compound. The area sealed with the sealing material is defined as a package body or sealing part 66. Advantageously, the downset or offset nature of the inner ends 30 of the leads 22 allows for the sealing part 66 to encompass that volume under the inner end bottom surface 82 for enhanced bonding of the leads 22.

[0044] In the embodiment shown, the chip mounting pad 18 is shown as not being downset and the resulting semiconductor package 12 is formed with the chip mounting pad 18 having an exposed mounting pad bottom surface 76. This is contemplated to have certain heat dissipation advantages. However, it is understood that the chip mounting pad 18 may be downset with respect to other portions of the lead frame 10 with the tie bars 20 having transitions sections (not shown). In this regard, the mounting pad bottom surface 76 may be surrounded with

sealing material.

[0045] Finally, the semiconductor package 12 is formed with the completion of a singulation process or step. In this respect, in the lead frame 10, the leads 22 are singulated to separate the semiconductor package 12 from the frame 14. Referring additionally to the completed semiconductor package 12 of Figures 5 and 7, as respectively seen along axes 5-5 and 7-7 of Figure 4, this results in the leads 22 including the distal ends 68 opposite the inner ends 30. The distal ends 68 each include an exposed end surface 70 and an exposed bottom surface or signal land 72. In this regard, the signal lands 72 are disposed about the periphery of the bottom surface of the semiconductor package 12. The semiconductor package 12 may be utilized in electrical communication with the printed circuit board by soldering the signal lands 72 directly to the printed circuit board. Similarly, the stub portion distal sections 58 may include exposed distal section bottom surfaces 90 for solder connection to the printed circuit board.

[0046] This disclosure provides exemplary embodiments of the present invention. The scope of the present invention is not limited by these exemplary embodiments. Numerous variations, whether explicitly provided for by the specification or implied by the specification, such as variations in structure, dimension, type of material and manufacturing process may be implemented by one of skill in the art in view of this disclosure.